An Introduction to Basic Research
on High-End Processor in China

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Agenda

● Background

● Our Research
  – Research Work Overview
  – Recent Papers

● Future Work
Processor Scaling Mismatches
Moore’s Law

- Moore’s Law is still in effect
- But processor microarchitecture does not scale well
  - Frequency scaling ends
  - Aggressive ILP exploitation becomes inefficient
  - Power dissipation meets limitation

→ Parallel Microprocessor
New Theory, New Architecture and New Methodology to Scale Microprocessor Design

- China Basic Research Project
  No. 2005CB321600 (fund: ¥ 35 million)

- Problems Formulation:
  3 Technology Walls for Future High-End Microprocessor
  - Information system complexity
  - Information processing energy consumption
  - Reliable information system
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Limited by power and complexity, superscalar processor is being replaced by on-chip multi-core / many-core processor.
Overview of Our Research Work

- Concluded as “1+2+N”
  - 1: scalable, configurable parallel microarchitecture
  - 2: multi-heavy-core (Loongson-3B) many-light-core (Godson-T)
  - N: a number of new theory, new architecture and new methodology to address the technology walls
Scalable and Configurable TGAP Architecture (Tera-op Godson Architecture Prototype)

- Scalable parallel microarchitecture
- Configurable on-chip network and memory
- Flexible resource isolation

![Diagram of Scalable and Configurable Architecture](image-url)
Exploiting Polymorphic Parallelism

Instruction-Level Parallelism

Godson-3

With Powerful Streaming Unit

Heterogenous Many-Core

Godson-T

With moderate DLP and strong TLP exploitation

Thread-Level Parallelism

Instruction-Level Parallelism

2012/1/5
Two High-Performance Microprocessor Prototypes

- **loongson3**: research on efficient heavy-core technology and nanometer IC design, test and verification
  - Loongson 3A: 4-core, 65nm, 1GHz, 16GFLOPS
  - Loongson 3B: 8-core, 65nm, 1GHz, 128GFLOPS
  - Loongson 3C: 16-core, 28nm, 1.5GHz, 384GFLOPS, tape out in 2011
- **Godson-T**: research on massively-parallel computing technology
  - 64 tiles, 4 memory controllers, sample (16 tiles) taped out now.
  - New technologies to handle memory latency and bandwidth, reliability, testability, etc.
Loongson-3A

- 4 four-issue 64-bit heavy-core in a node;
- High throughput I/O and memory controller are integrated;
- 65nm, 425 million transistors, 174mm$^2$, 1GHz, 10-watt
Loongson-3B

- 2 nodes, total 8 cores
- 128 GFLOPS provided by powerful streaming unit
- 65nm, 1GHz, 300mm²
Loongson-3C

- 4 nodes, 16 cores
- 128 64-bit FMADD units
- 1.5 GHz@32nm, 200mm²

- Peak Performance
  - DP: 384 GFLOPS
  - SP: 768 GFLOPS
  - 16-bit: 1.5TOPS
  - 8-bit: 3TOPS

- Target for computation-intensive applications, such as scientific computation, visual computation, ...
Godson-T Many-Core Prototype

- 64 light-weight processing tiles currently, 256 tiles in 2015
- 16-tile sample: 130nm, 230mm², SMIC
- Target for domain-specific parallel acceleration
Data-driven parallelism

Fast on-chip synchronization
Management

Efficient implicit/explicit memory management

Efficient task management

Fast and accurate simulation

Maximize parallelism exploitation

High-performance synchronization

High-performance communication

High-performance and easy-to-use task management

Research platform

Tape Out
3S: Self-Test, Self-Diagnosis, Self-Repair

- Reliable Design for Future Parallel Architecture
- Component failure will be normal in many-core processor, we use 3S to tolerate variety of abnormality including soft errors, intermittent faults and permanent faults. Keep service with 3S!

![Diagram of 3S components: Checkpoint, Self-Test, Self-Diagnosis, Self-Recovery, Self-Repair, with soft error, intermittent fault, and permanent fault]
Efficient mapping from virtual cores (seen from software) to physical cores

Repair defective cores with redundant cores

Increasing Godson-T chip yield through 3S
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Recent Papers – Partial Representative List

- LReplay: A Pending Period Based Deterministic Replay Scheme. ISCA 2010.
- DMA Cache: Using On-Chip Storage to Architecturally Separate I/O Data from CPU Data for Improving I/O Performance, HPCA 2010.
- Evaluating Iterative Optimization Across 1000 Data Sets. PLDI 2010.
- High Performance Comparison-Based Sorting Algorithm on Many-Core GPUs. IPDPS 2010.
- Fast Complete Memory Consistency Verification, HPCA 2009.

--- 2012/1/5
First work to model process, voltage and temperature variations as a uniform delay variation.

Efficiently address the fault prediction, detection and diagnosis problems.

Employ thread migration to prevent 50% voltage emergencies.
LReplay: A Pending Period Based Deterministic Replay Scheme (ISCA 2010)

- Hardware-based deterministic replay scheme facilitating global clock in a chip

- Result
  - Overall log size of LReplay Only generate 0.55B per kilo-instructions,
  - Very low hardware cost and easy to implement
High-throughput computing becomes more popular

- Computation-centric $\rightarrow$ Memory-centric $\rightarrow$ I/O-centric

I/O-centric microarchitecture

- Data is transferred between CPU and I/O via on-chip cache rather than memory
- Applied to Longson-3 chip, performance of SSD disk is improved by 40%
Propose a novel method that largely reduces the time complexity of processor memory consistency verification.

- Verification of 16-core Loongson-3 processor becomes feasible.
Most iterative optimization studies find the best optimizations on the same data set, which prevents its usage in practice.

We evaluated the effectiveness of iterative optimization across a large number (1000) of data sets.

Conclusion
- Compiler optimizations achieves 86% speedup than ICC (83% for GCC)
- optimizing programs across data sets much easier than previous anticipation

Figure 4. Reactions to compiler optimizations (adpcm_d).
High Performance Algorithm based on Novel Architecture (SPAA 2007)

- Optimized Dynamic Programming Algorithm is cited by Professor Vigaya Ramachandran (SPAA 2008 and Phd. Thesis directed by him)

A parallel algorithm for solving the parenthesis problem which..., but the algorithm is not cache-efficient. A cache-efficient multi-core algorithm for the IBM Cyclops64 processor was given in [25].

A similar algorithm for simple-DP is also given in [117], and in [118] the algorithm is extended for cache-efficient execution on a multicore programming model based on IBM Cyclops64.

The cache-oblivious stencil computation technique presented in [54] can be used as a dynamic programming algorithm for computing the length of a longest common subsequence of two sequences of length  \( n \) each in \( O(n^2) \) time, \( O(n) \) space and \( O\left(\frac{n^2}{B \ M}\right) \) I/Os. This method, however, does not compute the subsequence.
## Research Impact on Top-Tier Conferences

<table>
<thead>
<tr>
<th>Top-Tier Conference</th>
<th>Acceptance Rate</th>
<th># of Mainland Publishing</th>
<th># of ICT Publishing</th>
<th>Proportion</th>
<th>Notes</th>
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<tr>
<td>ISCA</td>
<td>18%</td>
<td>9</td>
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<td>HPCA</td>
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China’s new Nebulae Supercomputer is No. 2, right on the Tail of ORNL’s Jaguar in Newest TOP500 List of Fastest Supercomputers

Frit. 2010-05-28 00:31

Hamburg, Germany—China’s ambition to enter the supercomputing arena has become obvious with a system called Nebulae, built from a Dawning TC6600 Blade system with Intel X5550 processors and Nvidia Tesla C2050 GPUs. Nebulae is currently the fastest system worldwide in theoretical peak performance at 1.271 PFlops. With a Linpack performance of 1.271 PFlops, it holds the No. 2 spot on the 35th edition of the closely watched TOP500 list of supercomputers.

China’s new Nebulae Supercomputer holds No. 2 on Top 500
1.271 Petaflops

Godson-3 Emulates x86

The first presentation at the recent Hot Chips Symposium at Stanford University was the world’s first look at the Godson-3, the third generation of China’s most powerful microprocessor. It was the first time a Chinese CPU was to be shown to the US with hands-on instruction on new computer processor. China now occupies a major role in supercomputing and a major role in the supercomputer market. The new processor, based on Chinese programs, will be in the hands of research scientists in China and United States.

A Chinese Challenge to Intel

Researchers have revealed details of China’s latest homegrown microprocessor,

Tuesday, September 02, 2010

In California last week, China’s researchers unveiled details of a microprocessor that they hope will bring personal computing to most ordinary people in China by 2013. The new chip, code-named Godson-3, was developed with government funding by more than 200 researchers at the Chinese Academy of Sciences’ Institute of Computing Technology (ICT).

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Godson-3 introduction on “Microprocessor”

Godson-3 on MIT “Technology Review”

2012/1/5
Technology Transfer

- **Dawning supercomputers**
  - Occupied 27% in TOP100
  - Supercomputer in China (IBM 26%)
  - Contributions on oil exploration, national security, ...

- **Loongson microprocessors**
  - Set up Loongson Corp.
    (initial capital: about $ 30M)
  - Low-cost PC in China
    sell 150K units in Jiangsu
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Conventionally, HTC systems were implemented by HPC infrastructures. As requirements of throughput, energy-efficiency, scalability and reliability are increasing in emerging HTC systems, conventional wisdom is no longer suitable for next-generation data-center computing.
**Expected Contribution: HTC Microprocessor**

- **Kilo-Thread running on a chip**
  - To apply a new 973 project

<table>
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<tr>
<th>Processor</th>
<th># of Threads</th>
<th>Microarchitecture</th>
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<tr>
<td>AMD Opteron</td>
<td>12</td>
<td>12 cores</td>
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<tr>
<td>Intel Xeon</td>
<td>8</td>
<td>2~8 cores</td>
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<tr>
<td>Intel SCC</td>
<td>48</td>
<td>48 cores</td>
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<tr>
<td>IBM Power7</td>
<td>32</td>
<td>8 cores, 4-way multithreading</td>
</tr>
<tr>
<td>IBM Wire-Speed Processor</td>
<td>64</td>
<td>16 cores, 4-way multithreading, special-purpose hardware acceleration</td>
</tr>
<tr>
<td>Sun UltraSparc T2</td>
<td>64</td>
<td>8 cores, 8-way multithreading</td>
</tr>
<tr>
<td>Tilera TILEPro</td>
<td>64</td>
<td>64 cores</td>
</tr>
<tr>
<td><strong>HTC Processor of ICT</strong></td>
<td><strong>1024</strong></td>
<td><strong>1024 threads on a chip</strong></td>
</tr>
</tbody>
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Thanks